Claims

5   1. A processing unit (100) for processing a plurality of data streams by an
        algorithm divided into a plurality of Process Steps (PS), said processing unit
        (100) comprising:
        -an interconnection unit (102) comprising means for switching;
        -Process Step (PS) means (106) comprising at least two PS modules (106a-
10   106m), where each PS module (106a-106m) is connected to the
            interconnection unit (102) and a scheduler (110) connected to said
            interconnection unit (102) and to each PS module (106a-106m),
            characterised in that said processing unit (100) further comprises:
        -a memory unit (108) comprising at least two memories (108a-108n) wherein
15   each memory is connected to the interconnection unit (102);
        -the interconnection unit (102) further comprising means for providing at least a
            first connection between one of said memories and one of said PS modules
            and a second connection between another of said memories and another of
            said PS modules, wherein the interconnection unit (102) is adapted to
20   connect each memory to each of the PS modules by a switching activity,
            wherein the switching activity and the processing of the PS modules are
            controlled by the scheduler (110); and
        each memory (108a-108n) comprises means for storing a data stream and said
            stored data streams are manipulated in parallel by the connected PS
25   modules respectively, during a predetermined time period between said
            switching activities.

    2. Processing unit (100) according to claim 1, **characterised** in that said
        processing unit comprises at least one external memory (104) for storing at least
30   input and output data for the memories within the memory unit (108).

    3. Processing unit (100) according to claim 1, **characterised** in that said data
        streams are channels in a communication system.

4. Processing unit (100) according to claim 1, **characterised** in that said channels are speech channels and that said processing unit is implemented in a speech coder.

5. 5. Processing unit (100) according to claim 1, **characterised** in that said process step modules (106a-106m) are implemented by means of hardware suitable for the algorithm.

6. Processing unit (100) according to claim 1, **characterised** in that at least one of

10 the PS modules (106a-106m) transfer data between the external memory (104) and any of the memories within the memory unit (108).

7. A method for processing a plurality of data streams by an algorithm divided into a plurality of Process Steps (PS) by using an interconnection unit (102)

15 comprising means for switching, Process Step (PS) means (106) comprising at least two PS modules (106a-106m), each connected to the interconnection unit (102) and a scheduler (110) connected to said interconnection unit (102) and to each PS module (106a-106m), **characterised** in that the method comprises the steps of:

20 -*connecting* at least two memories (108a-108n) within a memory unit (108) to the interconnection unit (102);

-*providing* by the interconnection unit (102) a first connection between one of said memories and one of said PS modules and a second connection between another of said memories and another of said PS modules, wherein

25 the interconnection unit (102) is adapted to connect each memory to each of the PS modules by a switching activity, wherein the switching activity and the processing of the PS modules are controlled by the scheduler (110)

-*storing* a data stream in each memory, and

-*manipulating* said data streams in parallel by the connected PS modules

30 respectively, during a predetermined time period between said switching activities.

8. Method according to claim 7, **characterised** in that the method comprises the further step of:

35 -*storing* at least input and output data, for the memories within the memory unit (108), at the at least one external memory (104).

9. Method according to claim 7, **characterised** in that said data streams are channels in a communication system.

5   10. Method according to claim 9, **characterised** in that said channels are speech channels and that said processing unit (100) is implemented in a speech coder.

11. Method according to claim 7, **characterised** in that said process step modules (106a-106m) are implemented by means of hardware suitable for the algorithm.

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12. Method according to claim 7, **characterised** in that at least one of the PS modules transfers data between the external memory (104) and any of the memories within the memory unit (108).

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